WHAT IS CLAIMED IS:

1. A transceiver apparatus for use in a portable wireless communication terminal, comprising:

a transceiver section for supporting wireless communication operations of the portable wireless communication terminal, including an input to which at least a portion of said transceiver section is responsive for entering either of a powered-down state and a powered-up state; and

a timing sequencer coupled to said input for signaling said transceiver section to enter said powered-up and powered-down states in a desired sequence to perform a desired operation, said timing sequencer including an input for receiving from a baseband processor a signal requesting the desired operation, said timing sequencer responsive to the baseband processor signal for signaling said desired power-up/power-down sequence to said transceiver section without requiring further signaling from the baseband processor.

2. The apparatus of Claim 1, including a frequency generator coupled to said transceiver section for providing a frequency signal to said transceiver section, said timing sequencer coupled to said frequency generator for receiving therefrom information

indicative of whether said frequency generator has achieved a locked state, said timing sequencer selectively responsive to said locked state information for signaling said transceiver section to enter said powered-up state.

3. The apparatus of Claim 2, wherein said frequency generator has an input for receiving said baseband processor signal, said frequency generator responsive to said baseband processor signal for leaving a powered-down state thereof and entering a powered-up state thereof, said timing sequencer coupled to said frequency generator for signaling said frequency generator to leave said powered-up state thereof and enter said powered-down state thereof.

4. The apparatus of Claim 2, wherein said timing sequencer includes a lock delay timer coupled to said timing sequencer input and responsive to said baseband processor signal for tracking a delay time during which said frequency generator is expected to achieve said locked state, said timing sequencer further including a lock detector coupled to said lock delay timer and said frequency generator, said lock detector responsive to expiration of said delay time for detecting from said frequency generator

locked state information whether said frequency generator has achieved said locked state, said lock detector responsive to detection of said locked state for signaling said transceiver section to enter said powered-up state.

5. The apparatus of Claim 4, including a serial programming interface coupled to said lock delay timer for permitting the baseband processor to program said delay time into said lock delay timer.

6. The apparatus of Claim 4, wherein said timing sequencer includes a transceiver timer coupled to said lock detector and responsive to detection of said locked state for tracking a further delay time associated with operation of said transceiver section, said transceiver timer responsive to expiration of said further delay time for signaling said transceiver section to enter said powered-down state.

7. The apparatus of Claim 2, wherein said timing sequencer includes a transceiver timer responsive to said locked state information for tracking a delay time associated with operation of said transceiver section, said transceiver timer responsive to

expiration of said delay time for signaling said transceiver section to enter said powered-down state.

8. The apparatus of Claim 7, including a serial programming interface coupled to said transceiver timer for permitting the baseband processor to program said delay time into said transceiver timer.

9. The apparatus of Claim 1, including a selection apparatus coupled between said timing sequencer and said transceiver section input for selecting one of said timing sequencer and the baseband processor for connection to said transceiver section input.

10. The apparatus of Claim 9, including a serial programming interface coupled to said selection apparatus for permitting the baseband processor to program the desired selection into said selection apparatus.

11. The apparatus of Claim 1, wherein said timing sequencer includes a programmable state machine.

12. The apparatus of Claim 11, including a serial programming interface coupled to said programmable state machine for permitting the baseband processor to program said programmable state machine.

13. The apparatus of Claim 1, provided on a single integrated circuit.

14. A transceiver apparatus for use in a portable wireless communication terminal, comprising:

a transceiver section for supporting wireless communication operations of the portable wireless communication terminal;

a frequency generator having an output coupled to said transceiver section for providing thereto a frequency signal;

a plurality of registers coupled to said frequency generator, each of said registers for storing therein information indicative of a respective one of a plurality of frequencies to which said frequency signal is to be sequentially shifted; and

an input for coupling to a baseband processor of the portable wireless communication terminal to receive therefrom information indicative of a desired sequence of frequencies through which said frequency signal is to be shifted, said registers coupled to said input and responsive to said desired sequence information for providing their respective frequency information to said frequency generator sequentially according to said desired sequence.

15. The apparatus of Claim 14, wherein said input is connected to said registers for permitting the baseband processor to directly access said registers sequentially using said desired sequence information.

16. The apparatus of Claim 14, including a register accessor coupled between said input and said registers, said register accessor responsive to said desired sequence information for accessing said registers sequentially according to said desired sequence.

17. The apparatus of Claim 16, wherein said register accessor includes further registers for respectively storing therein information indicative of respective sequences of frequencies through which said frequency signal can be shifted, said register accessor including an access sequencer coupled to said further registers for receiving from said further registers said stored frequency sequence information, said access sequencer responsive to said received frequency sequence information for accessing said first-mentioned registers sequentially according to said received frequency sequence information.

18. The apparatus of Claim 17, wherein said register accessor is responsive to said desired sequence information for accessing one of said further registers corresponding to said desired sequence and for loading said access sequencer with the frequency sequence information stored in said one of said further registers.

19. The apparatus of Claim 18, wherein said register accessor includes a decoder coupled between said input and said further registers for decoding said desired

sequence information to produce information indicative of said one of said further registers that is to be accessed for loading said access sequencer.

20. The apparatus of Claim 17, including a serial programming interface coupled to said further registers for permitting the baseband processor to load said frequency sequence information into said further registers.

21. The apparatus of Claim 17, wherein said access sequencer includes a programmable state machine that is programmable with said frequency sequence information.

22. The apparatus of Claim 16, wherein said register accessor includes a programmable state machine that is connected to said input and is programmable with said desired sequence information.

23. A method of controlling a transceiver section provided on a transceiver side of a portable wireless communication terminal that also includes a baseband side coupled to the transceiver side, comprising:

receiving on the transceiver side a signal from the baseband side requesting a desired transceiver operation; and

in response to said requesting signal from the baseband side, signaling at least a portion of the transceiver section to enter a powered-up state thereof and a powered-down state thereof in a desired sequence, including generating on the transceiver side signaling that produces the desired power-up/power-down sequence without requiring further signaling from the baseband side.

24. The method of Claim 23, including enabling a frequency generator in response to said requesting signal from the baseband side, waiting for a first predetermined amount of time after enabling the frequency generator, and determining, after expiration of the first predetermined amount of time, whether the frequency generator has achieved a locked state.

25. The method of Claim 24, wherein said generating step includes, in response to a determination that the frequency generator has achieved a locked state, generating a signal that drives the transceiver section into said powered-up state thereof, waiting for a second predetermined amount of time, and generating, after expiration of the second predetermined amount of time, a signal that places the transceiver section into said powered-down state thereof.

26. A method of controlling a frequency generator provided on a transceiver side of a portable wireless communication terminal that also includes a baseband side coupled to the transceiver side, comprising:

storing on the transceiver side information indicative of a plurality of frequencies to which a frequency signal output of the frequency generator is to be sequentially shifted;

thereafter, receiving on the transceiver side from the baseband side information indicative of a desired sequence of frequencies through which said frequency signal is to be shifted; and

responsive to said desired sequence information, using the stored frequency information to shift said frequency signal through the desired sequence of frequencies.

27. The method of Claim 26, wherein said stored frequency information includes divisors for use in a feedback loop of a PLL, said using step including sequentially loading the divisors into the feedback loop.

28. The method of Claim 26, wherein said stored frequency information includes radians per clock cycle values for use in a DDFS, said using step including sequentially loading the values into the DDFS.

29. The method of Claim 26, including storing on the transceiver side information indicative of sequences of frequencies through which said frequency signal can be shifted, said using step including using said stored frequency information and said stored frequency sequence information to shift said frequency signal through the desired sequence of frequencies.

30. The method of Claim 29, wherein said last-mentioned using step includes accessing said stored frequency information in response to said stored frequency sequence information.

31. The apparatus of Claim 1, wherein said frequency generator includes a phase locked loop(PLL).

32. The apparatus of Claim 1, wherein said frequency generator includes a direct digital frequency synthesizer (DDFS).

33. The apparatus of Claim 14, wherein said frequency generator includes a phase locked loop (PLL).

34. The apparatus of Claim 14, wherein said frequency generator includes a direct digital frequency synthesizer (DDFS).